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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,702	12/27/2001	Sean-Paul Woyciehowsky	MULT1807	8595

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,702	WOYCIEHOWSKY ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14 and 15* is/are allowed.

6)☒ Claim(s) *1-7,12 and 13* is/are rejected.

7)☒ Claim(s) *8-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuhara U.S. Patent 6,075,825.

Regarding claim 1, Mizuhara invention is directed to a timing and data recovery circuit in a receiver. Referring to figure 2, in column 3 lines 8-50, figure 2 illustrates a data and timing recovery circuit 30, which corresponds to the claimed clock and data recovery apparatus. The data and timing recovery circuit 30 includes:

A nonlinear circuit 36 for detecting the timing information from the data stream; the output of nonlinear circuit 36 fed to a low Q bandpass filter 38 for extracting the clock signal; output from the low Q bandpass filter 38 fed to a clock divider 40 that divides the clock speed by n to slow the clock signal down. In light of the forgoing disclosure, the Q bandpass filter 38 and clock divider 40 perform the means function specified in the claim. As result of that, one of ordinary skill in the art would have recognized that the interchangeability of the elements taught in Mizuhara invention for the corresponding means for deriving and dividing a clock signal as set forth in the claim.

The output of clock divider 40 is fed to a high Q band-pass filter 42 to reduce timing jitter before being sent on to a plurality of decision circuits 44a, 44b, ..., 44n, where data signal is recovered from the input data stream; see column 3, lines 30-37. Mizuhara invention does not expressly teach the claimed limitations "*means for retiming the incoming data and for multiplexing the retimed data to regenerate the incoming data*". As recited above, the decision circuits 44a, 44b, ..., 44n are enabled by the recovered clock to retime the data signal from the input data stream. In light of that, one of ordinary skill in the art would have recognized that the interchangeability of the decision circuits 44a, 44b, ..., 44n taught by Mizuhara for the corresponding means for enabled by the divided clock signal for retiming the incoming data as set forth in the claim.

Regarding claim 2, as recited in claim 1, the low Q bandpass filter 38 is for extracting the clock signal from the input data stream. Hence, the low Q bandpass filter 38 corresponds to the claimed wave-guide filter apparatus.

2. Claims 3-7, 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuhara U.S. Patent 6,075,825 as applied to claim 1 and further in view of Davis U.S. Patent 3,992,581.

Regarding claim 3, Mizuhara does not employ an amplifier coupled with the low Q bandpass filter 38 as set forth in the claim. Davis invention is directed to a phase locked loop repeater for reshaping a non return zero (NRZ) data stream. Referring to

figure 1, column 3, lines 2-35, the incoming NRZ encoded data is applied to a transistor detector 22 to produce discreet pulse each time the incoming signal rises above or drops below a predetermined threshold. The discreet pulse is then applied to a first input of a phase detector network 26 whose output is amplified by means of an integrating amplifier 30. Mizuhara and Davis teachings are in the same field of endeavor. Davis invention differs from Mizuhara in that Davis repeater employs a PLL for reshaping and retiming NRZ data stream. Nevertheless, utilization of amplifier as taught by Davis is just for amplifying the recovered clock, one of ordinary skill in the art would have been motivated to use an amplifier in Mizuhara timing and data recovery circuit for amplifying the clock signal. The utilization of an amplifier is known in the art for amplifying weak signal for further processing.

Regarding claim 4, referring to figure 3 of Mizuhara invention, the data and retiming recovery circuit employs a clock divider 60 for dividing the clock speed by 2 and generating the divided clock signal. The clock divider 60 corresponds to the claimed frequency divider.

Regarding claim 5, Mizuhara does not teach utilization of an amplifier connected to the frequency divider as set forth in the claim. Nevertheless, Mizuhara discusses a prior art in figure 1, wherein the prior art employs a limiting amplifier 20 to suppress the AM component of the clock signal; see column 2, lines 54-67. Using analogous argument as recited in claim 3, because utilization of an amplifier as taught in prior art is

just for amplifying the recovered clock, one of ordinary skill in the art would have been motivated to use an amplifier in Mizuhara timing and data recovery circuit for amplifying the clock signal. The utilization of an amplifier is known in the art for amplifying weak signal for further processing, and for suppressing the AM component of the clock signal due to the NRZ data pattern effect as taught in prior art. With the combined teachings, output from the limiting amplifier is an amplified divided clock signal.

Regarding claim 6, referring to figure 2 of Mizuhara invention, output from the high Q BPF 42 is applied to a plurality of decision circuits 44a, 44b, ..., 44n, where the data signal is recovered from the input data stream; see column 3, lines 30-40. In light of the foregoing, decision circuits 44a, 44b, ..., 44n, corresponding to the claimed decision means, receives the incoming NRZ data and enabled by the divided clock signal and for multiplexing the generated data with the divided clock signal to generate the incoming data, see figure 2.

Regarding claim 7, Mizuhara does not teach a phase shifter as set forth in the application claim. Nevertheless, as expressly taught in Mizuhara invention, the high Q band-pass filter 42 reduces timing jitter before sending the clock signal to the plurality of decision circuits 44a, 44b, ..., 44n. In view of that, the high Q band-pass filter 42 performs an equivalent function of a phase shifter to time align the decision circuits 44a, 44b, ..., 44n. As result of that, a person of average skill in the art would have

recognized that the interchangeability of the high Q band-pass filter 42 taught in Mizuhara invention for the corresponding phase shifter as set forth in the claim.

Regarding claim 12, claim 12 is rejected on the same ground as for claim 7 because of similar scope.

Regarding claim 13, claim 13 is rejected on the same ground as for claim 7 because of similar scope. Referring to figure 2, the timing and data recovery circuit 10 further includes a nonlinear circuit 36, which receives the incoming non-return zero input data and detects from the timing information from the data stream. In light of the aforementioned teachings, the nonlinear circuit 36 generates pseudo data from the incoming non-return zero data as appreciated by one of ordinary skill in the art.

Allowable Subject Matter

3. Claims 8-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 14-15 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 14-15, claims 14-15 are allowable over the prior art of record since the cited references taken individually or in combination fails to particularly disclose a clock and data recovery apparatus for recovering and regenerating incoming return to zero data, the clock and data recovery apparatus comprising "*a pair of flip-flop circuits doubled triggered by the incoming data and by the divided clock signal and a complimentary of the divided clock signal for generating data at a data rate reduced by one-half of the data rate of the incoming return to zero data*" and "*a multiplexer apparatus connected to the pair of flip-flop devices for receiving the generated reduced rate data and controlled by the divided clock signal for regenerating the return-to-zero incoming data from the reduced rate data*". It is noted the closest prior art, Mizuhara (US 6,075,825) disclosing Timing And Data Recovery Circuit For Ultra High Speed Optical Communication System and Thomas et al. (US 4,996,444) disclosing a clock recovery circuit, fail to anticipate or render the above underlined limitations obvious.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Davis U.S. Patent 3,992,581 discloses "Phase Locked Loop NRZ Data Repeater".

Dalmia et al. U.S. Patent 6,307,413 discloses "Reference-Free Clock Generator And Data Recovery PLL".

Tamamura et al. U.S. Patent 6,118,316 discloses "Semiconductor Integrated Circuit Including Plurality Of Phase Locked Loops".

Pedrotti et al. U.S. Patent 6,643,346 discloses "Frequency Detection Circuit For Clock Recovery".

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

Khanh cong Tran 03/04/2005

Examiner KHANH TRAN